LISTING OF THE CLAIMS

1-79. (Cancelled).

80. (Currently Amended) A method of operating an active pixel CMOS imager, comprising:

activating a first pixel in a row of pixels connected to a shared column line ~~for a first period of time~~ and then subsequently activating an adjacent second pixel in the row of pixels connected to the shared column line ~~for a second period of time~~, ~~the array comprising~~ the first and second pixels disposed in a pixel array;

~~detecting a first voltage level at a node of the first pixel;~~

resetting ~~the first~~ a voltage level of ~~the~~ a node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array;

transferring charge collected by the first pixel to the node;

detecting the charge at the node; and

generating an output signal over the shared column line corresponding to the charge detected at the node.

81. (Previously Presented) The method of claim 80, wherein the shared column line extends approximately linearly across the pixel array.

82. (Previously Presented) The method of claim 81, further comprising a row select line that extends approximately linearly across the pixel array.

83. (Previously Presented) The method of claim 80, further comprising a row select line that extends approximately linearly across the pixel array.

84. (Currently Amended) A method of operating a system, comprising:

focusing an image on an active pixel CMOS imager, the imager comprising a pixel array;

activating a first pixel in a row connected to a shared column line and then subsequently activating an adjacent second pixel in the row connected to the shared column line, the pixel array comprising the first and second pixels;

~~detecting a first voltage level at a node associated with the first pixel;~~

resetting ~~the first~~ a voltage level of ~~the~~ a node associated with the first pixel to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array;

transferring charge collected by the first pixel to the node;

detecting the charge at the node; and

generating an output signal over the shared column line, the output signal corresponding to the image.

85. (Previously Presented) The method of claim 84, wherein the shared column line extends approximately linearly across the pixel array.

86. (Previously Presented) The method of claim 85, further comprising a row select line that extends approximately linearly across the pixel array.

87. (Previously Presented) The method of claim 84, further comprising a row select line that extends approximately linearly across the pixel array.

88. (Previously Presented) An active pixel CMOS imager, comprising:

a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array;

a plurality of column lines each connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal;

a plurality of odd row select lines orthogonal to the column lines to address odd pixels in the rows;

a plurality of even row select lines orthogonal to the column lines to address even pixels in the rows;

a column driver to address pixels connected to the column lines; and

a row driver to address pixels through the odd row select lines and the even row select lines.

89. (Previously Presented) The imager of claim 88, wherein the column lines extend approximately linearly across the array.

90. (Previously Presented) The imager of claim 89, wherein the odd and even row select lines extend approximately linearly across the array.

91. (Previously Presented) The imager of claim 88, wherein the odd and even row select lines extend approximately linearly across the array.

92. (Previously Presented) The imager of claim 88, further comprising a plurality of reset lines that extend approximately linearly across the array.

93. (Currently Amended) A method of operating a CMOS imager, comprising:

addressing even pixels in a row of pixels of an array of pixels using a row driver coupled to an even row select line;

providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels;

addressing odd pixels in the row of pixels via an ~~even~~ odd row select line; and

providing a second output signal associated with light detected by the odd pixels to the plurality of column lines coupled to the odd pixels.

94. (Previously Presented) The method of claim 93, wherein the column lines extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line.

95. (Previously Presented) The method of claim 94, wherein the odd and even row select lines extend approximately linearly across the array.

96. (Previously Presented) The method of claim 94, further comprising a plurality of reset lines that extend approximately linearly across the array.

97. (New) An imaging device, comprising:

a row comprising a first pixel and a second pixel;

the first and second pixels being joined by a diagonal active area component;

an even row line connected with the first pixel;

an odd row line connected with the second pixel; and

a column line connected with the first and second pixels at the diagonal active area component.

98. (New) The imaging device of claim 97, wherein the row further comprises a plurality of first pixels and a plurality of second pixels.

99. (New) The imaging device of claim 97, wherein the even row line and odd row line extends substantially linearly across an array of pixels.

100. (New) The imaging device of claim 97, further comprising a first reset line for the first pixel and a second reset line for the second pixel.

101. (New) The imaging device of claim 100, wherein each of the even row line, odd row line, first reset line, and second reset line extend substantially linearly across the first and second pixels.

102. (New) An imaging device, comprising:

a pixel array comprising a row comprising a plurality of first pixels and a plurality of second pixels;

a first row address line connected with the first pixels;

a second row address line connected with the second pixels;

a respective column line for each pair of first and second pixels of the row; and

a reset line connected to the plurality of first pixels.

103. (New) The imaging device of claim 102, wherein the plurality of first pixels are every other pixel in the row.

104. (New) The imaging device of claim 102, wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line.

105. (New) The imaging device of claim 102, wherein each pair of first and second pixels are connected by a substantially diagonal active area.

106. (New) An imaging device comprising:

a row of pixels comprising a first address line connected to a first plurality of said pixels and a second address line connected to a second plurality of said pixels;

a plurality of read-out lines, each of said read-out lines being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels;

a reset line connected to at least the first plurality of pixels or the second plurality of pixels.